

Fig. 1

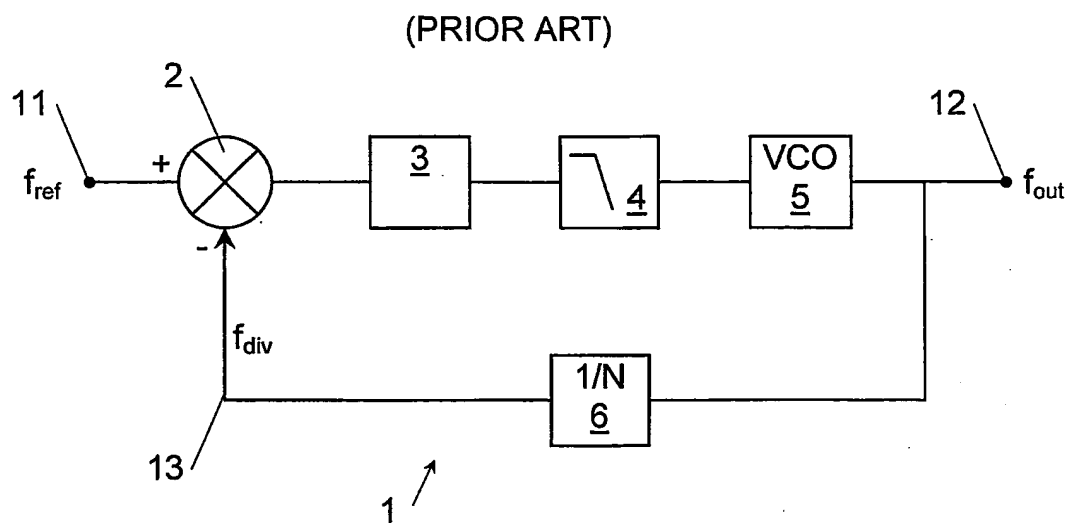


Fig. 2

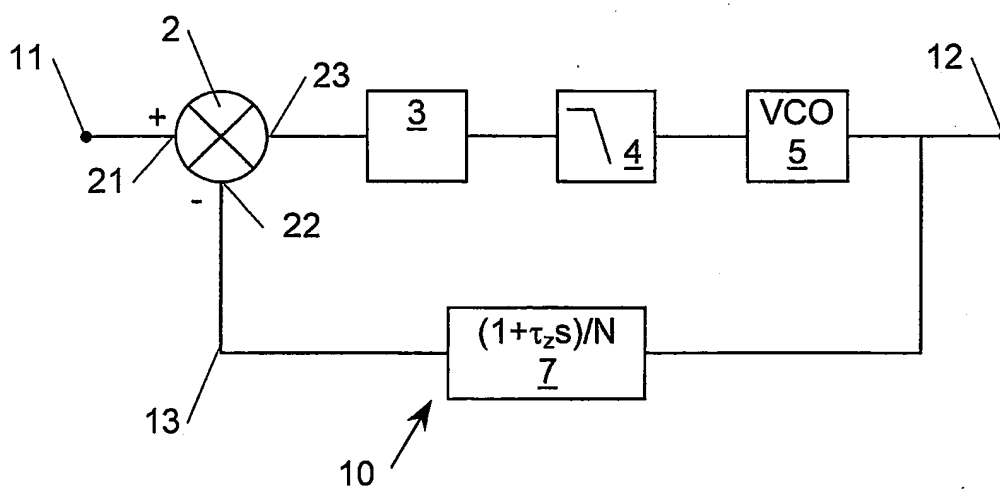


Fig. 3

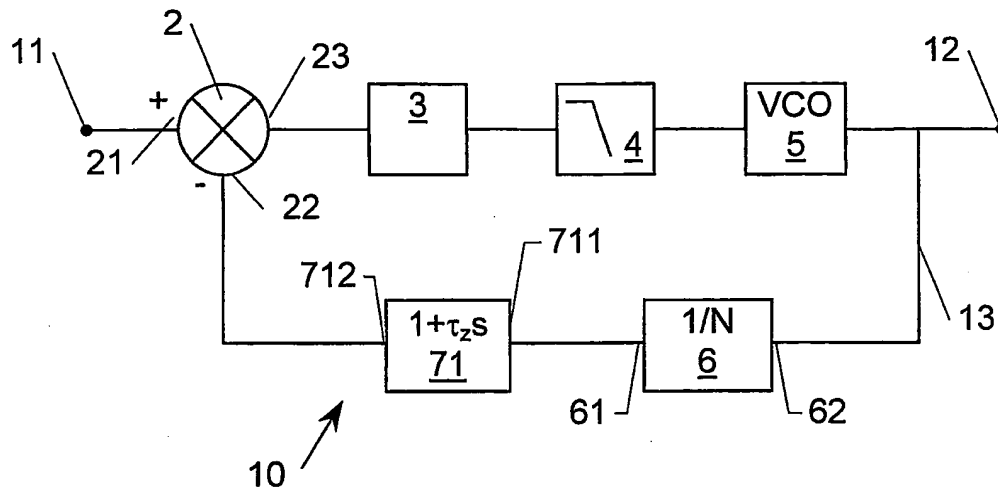
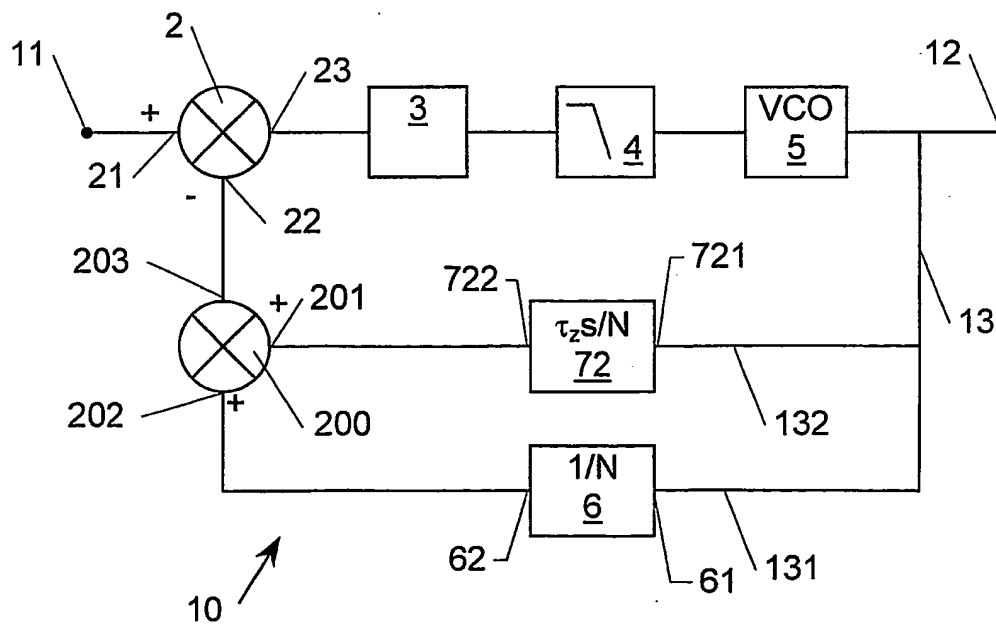


Fig. 4



The diagram shows a PLL system with a feedforward path. The main feedback loop consists of a phase detector (21) with inputs 11 and 22, a loop filter (23), a voltage-controlled oscillator (VCO 5), and a frequency divider (6) with gain 1/N. The output of the divider is 12, which is fed back to the phase detector. A feedforward path branches off from the output of the loop filter (23) and passes through a feedforward filter (73) with gain  $K_D \tau_z s / N$  before being fed back to the phase detector. The feedforward filter is composed of a zero-pole-pole-zero configuration (4) and a gain block (3). The overall system is labeled 10.

The diagram shows a PLL system. An input signal 11 is connected to a summing junction 21. The output of this junction is signal 23, which passes through a divider block 3 and a delay block 4 to become signal 12. Signal 12 is also connected to a VCO block 5. The output of the VCO is signal 13, which is fed back to a second summing junction 201. Signal 13 also branches off to a feedback path containing a delay block 721 and a sigma-delta modulator block 8. The output of the sigma-delta modulator is signal 63, which passes through a divider block 6 to become signal 61. Signal 61 is fed back to the second summing junction 201. The output of the second summing junction is signal 200, which passes through a delay block 722 and a divider block 62 to become signal 203. Signal 203 is fed back to the first summing junction 21. The output of the VCO 5 is also connected to a delay block 132, which feeds back to the second summing junction 201.

Fig. 7

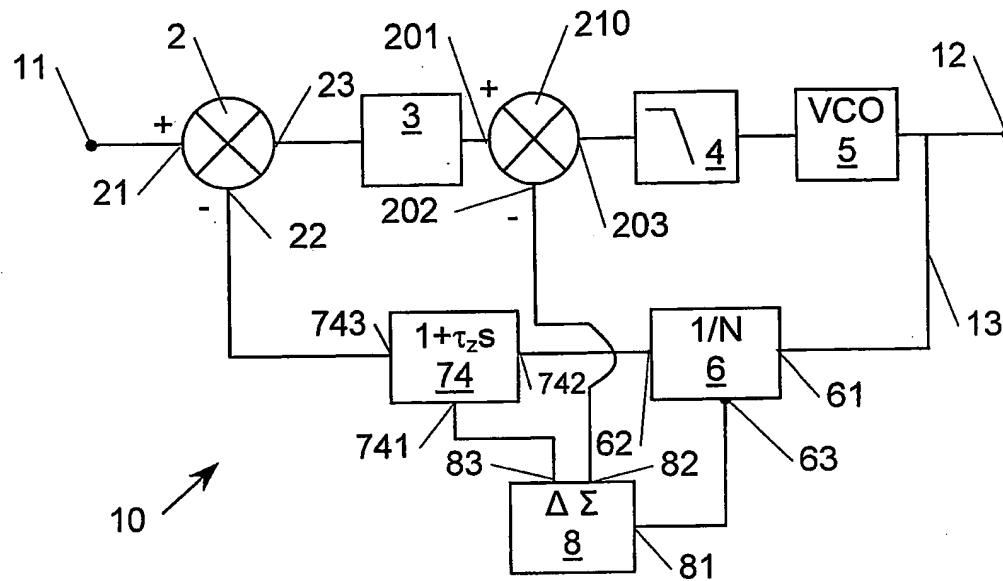


Fig. 8

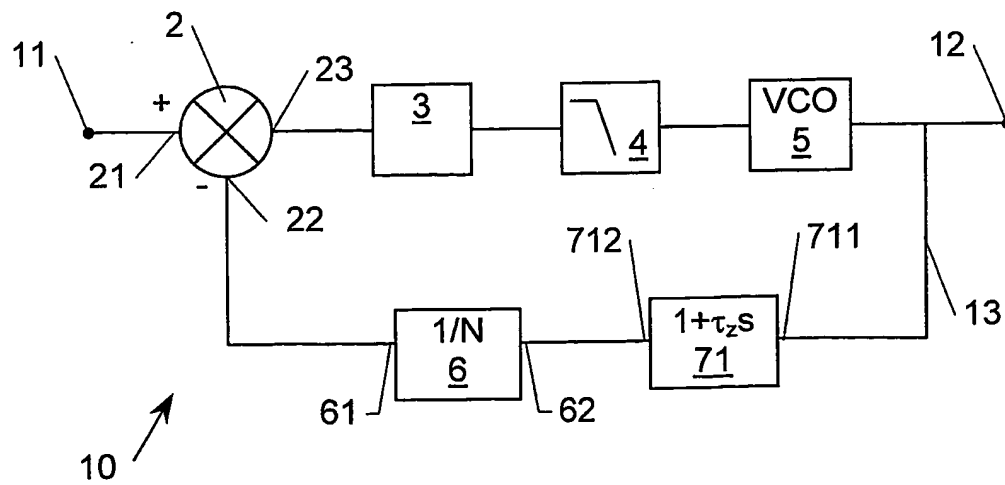


Fig. 9

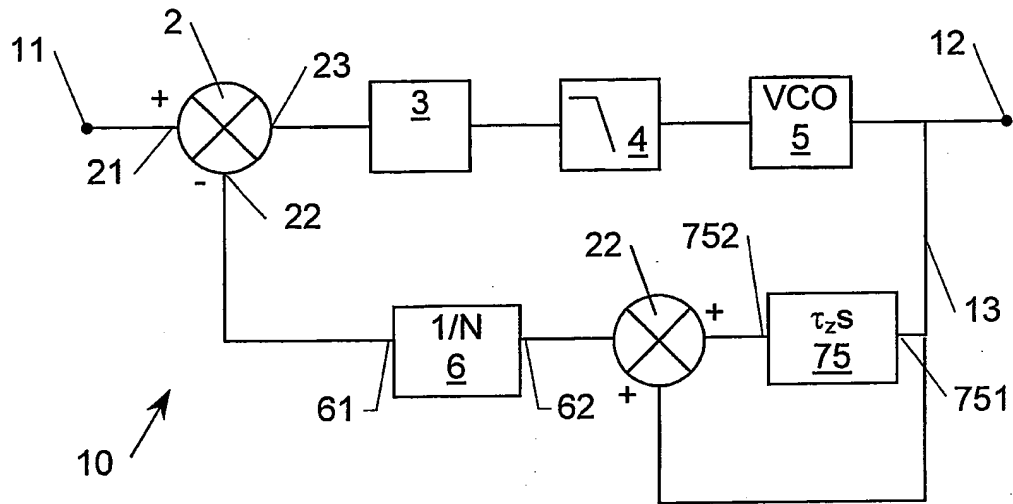


Fig. 10

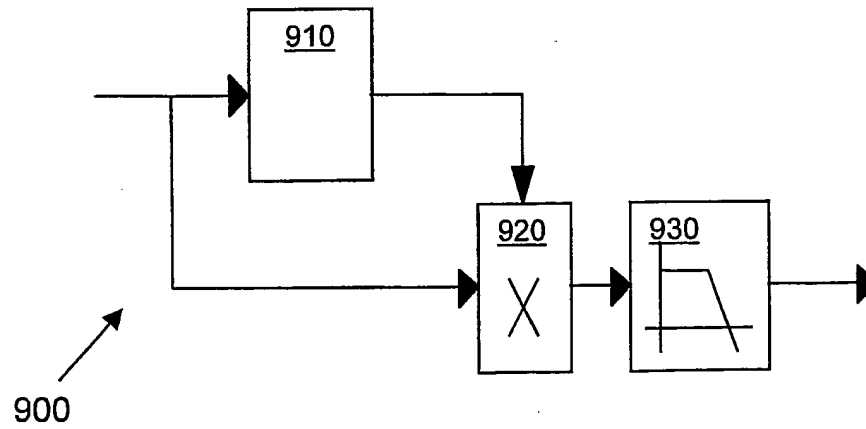


Fig. 11

